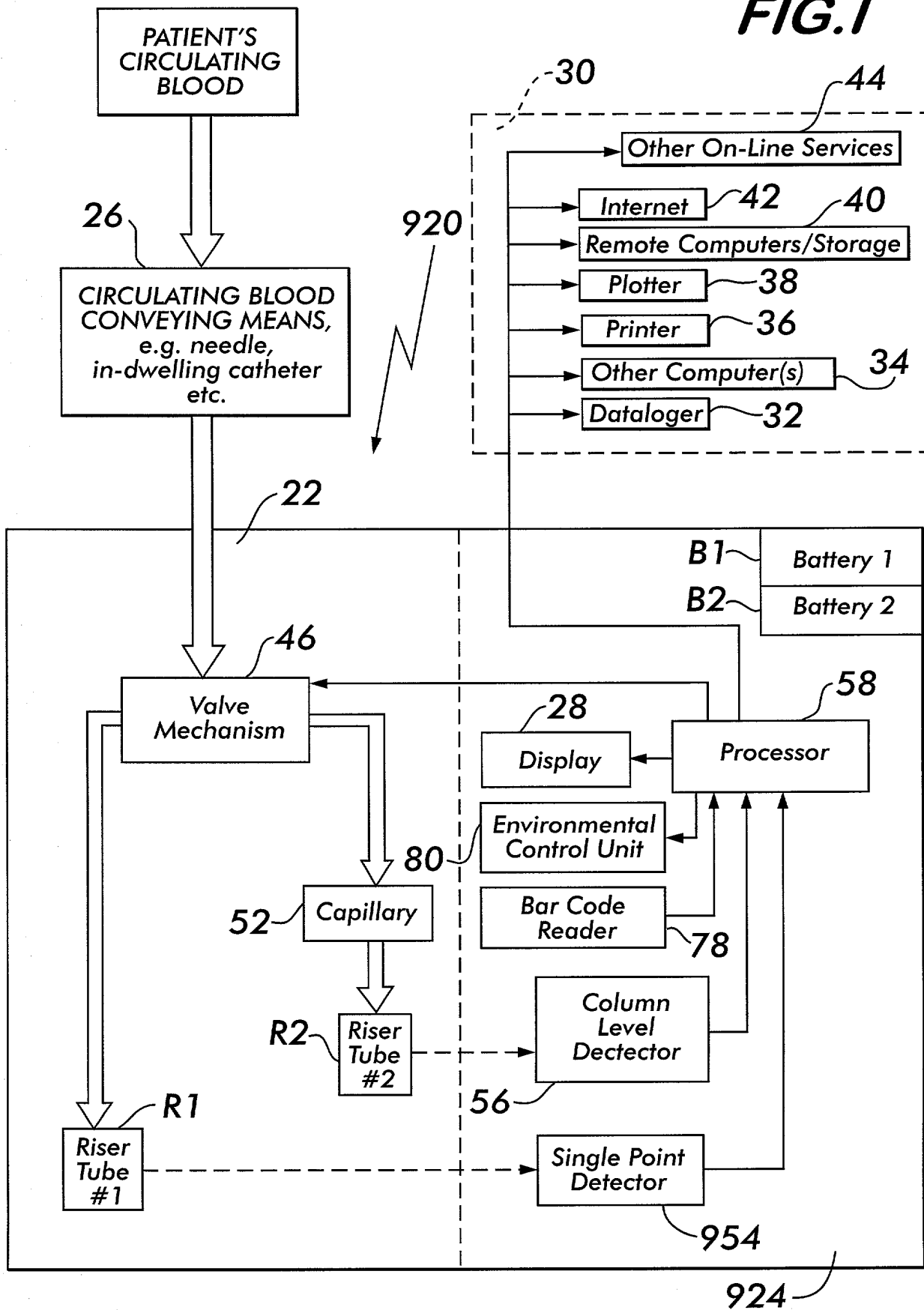
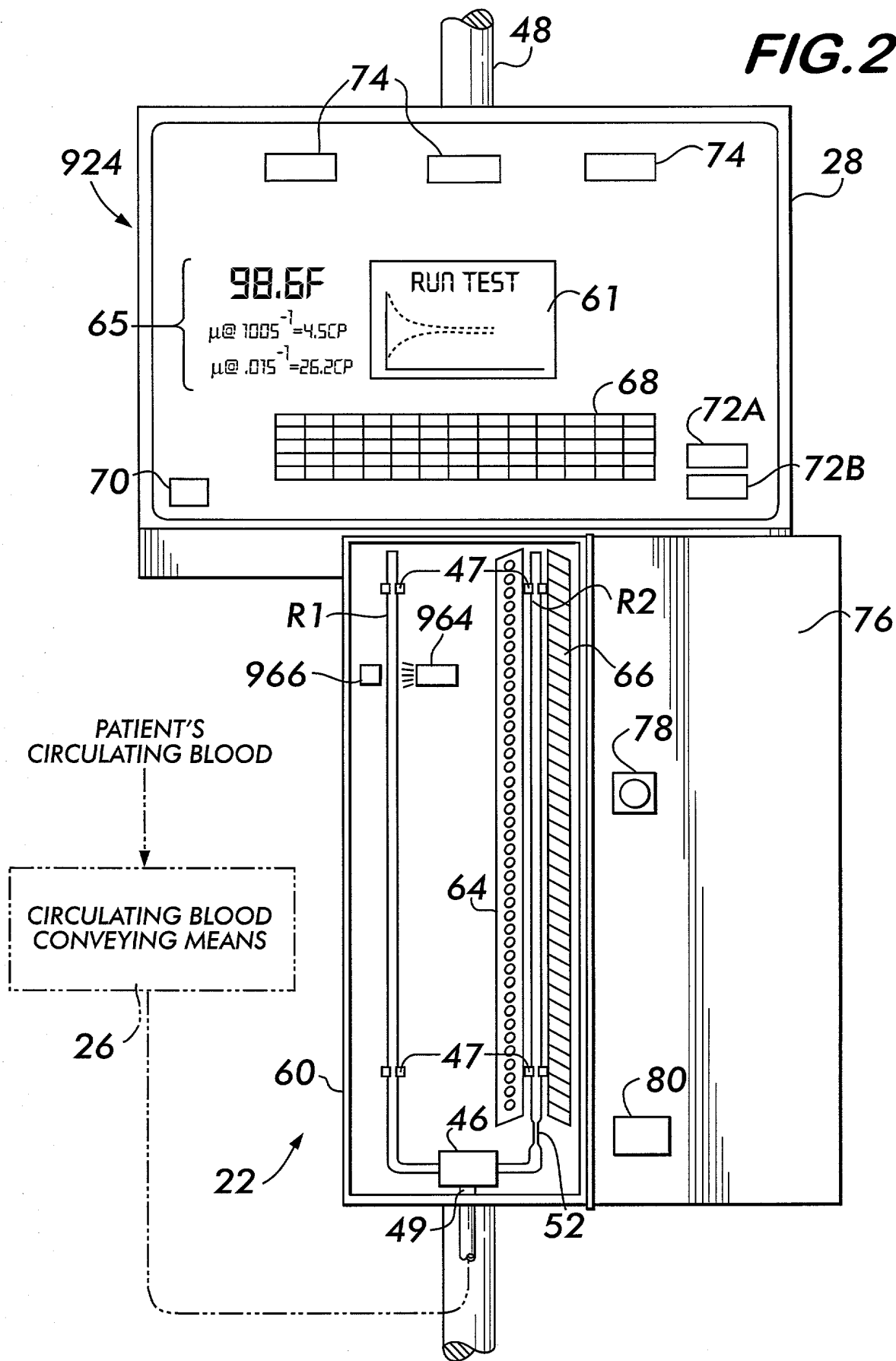


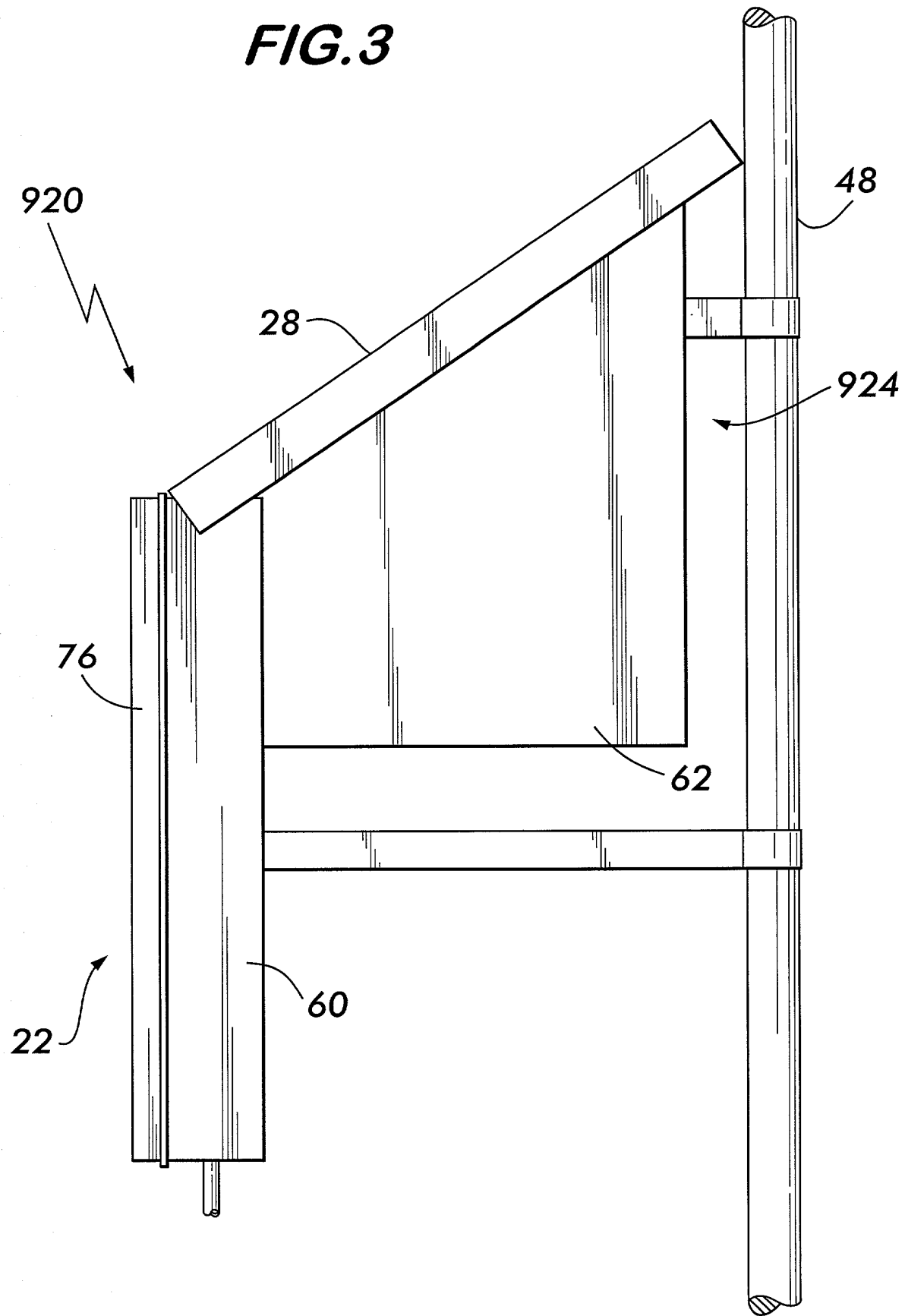
# FIG. 1



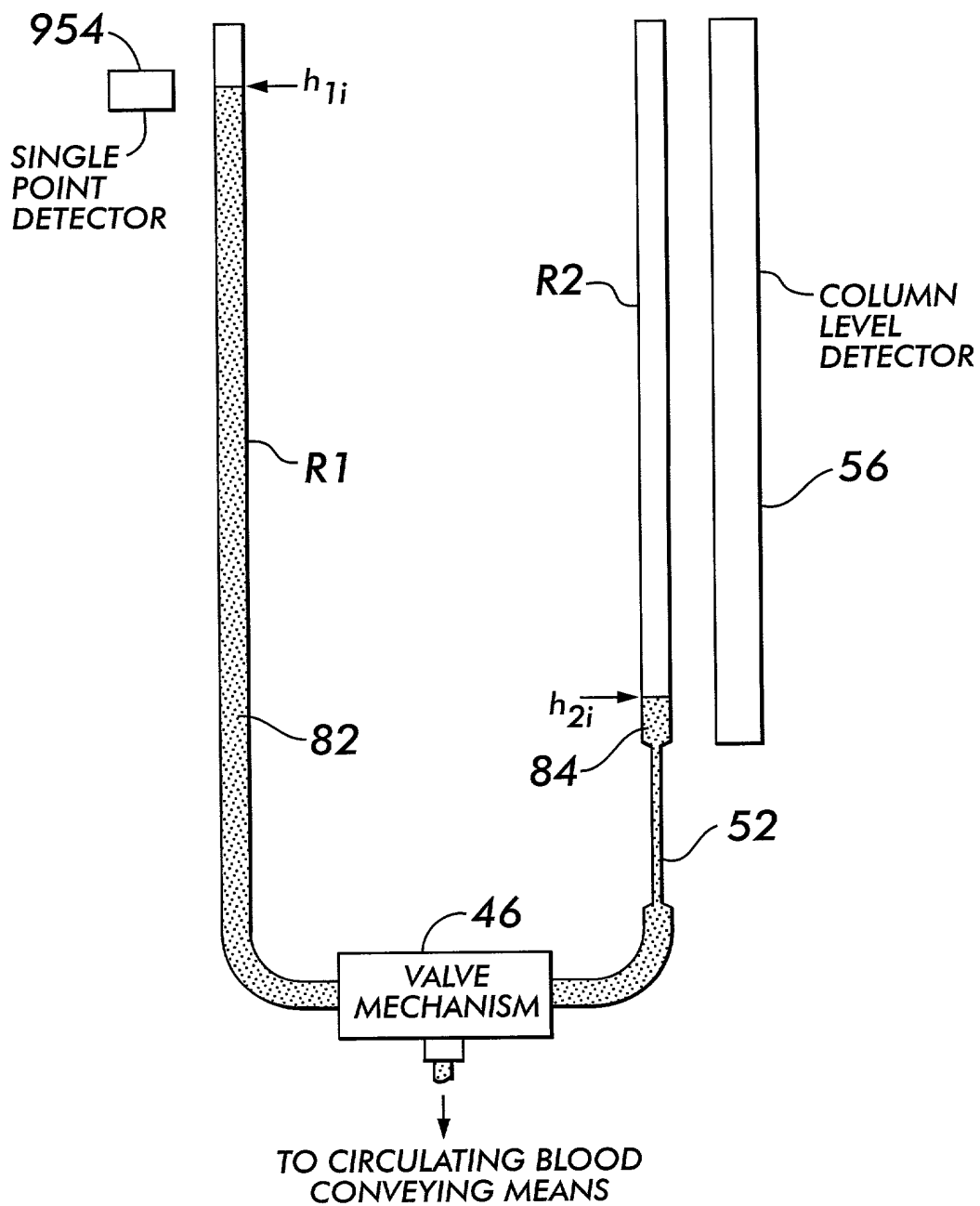
**FIG. 2**



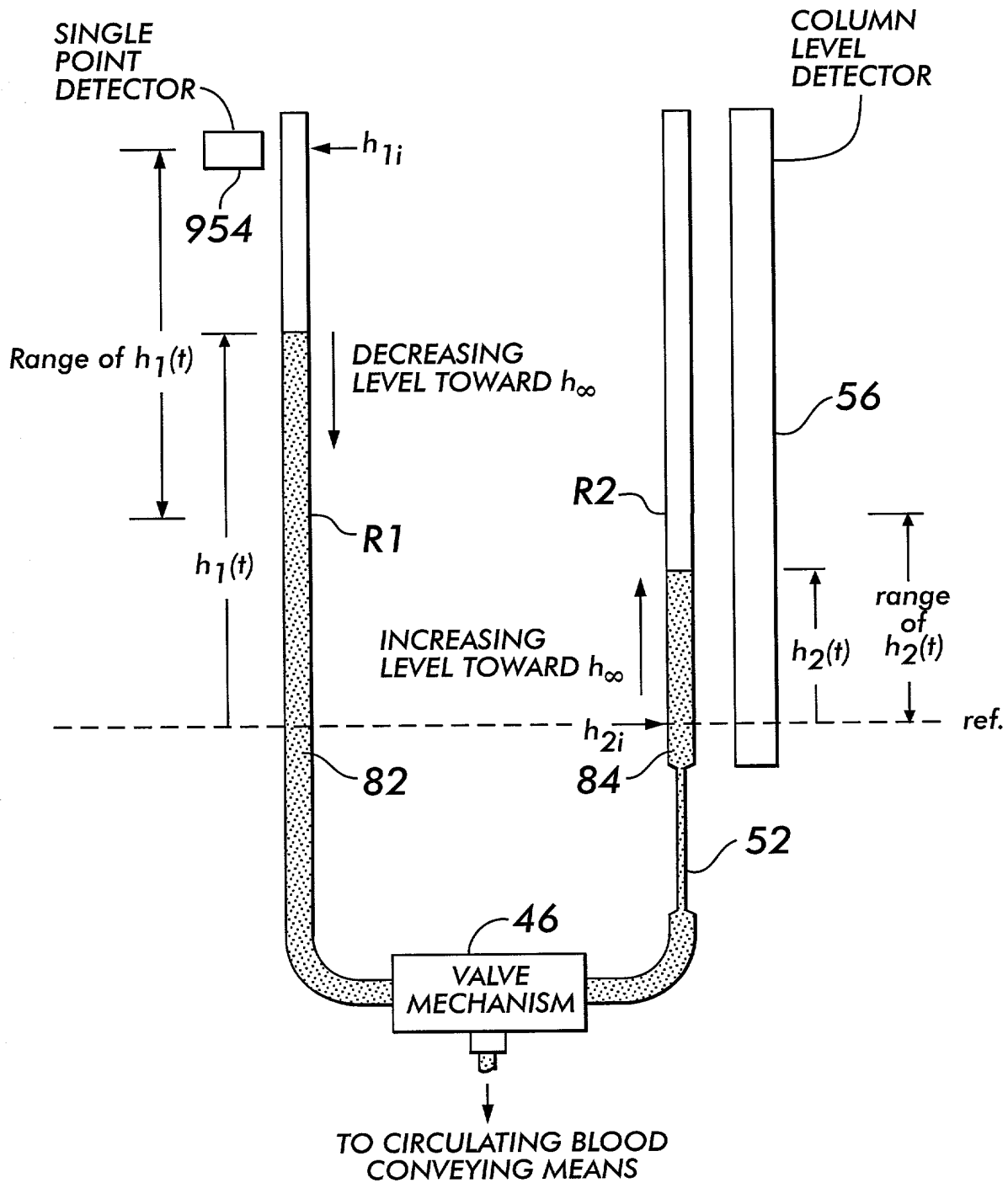
**FIG. 3**



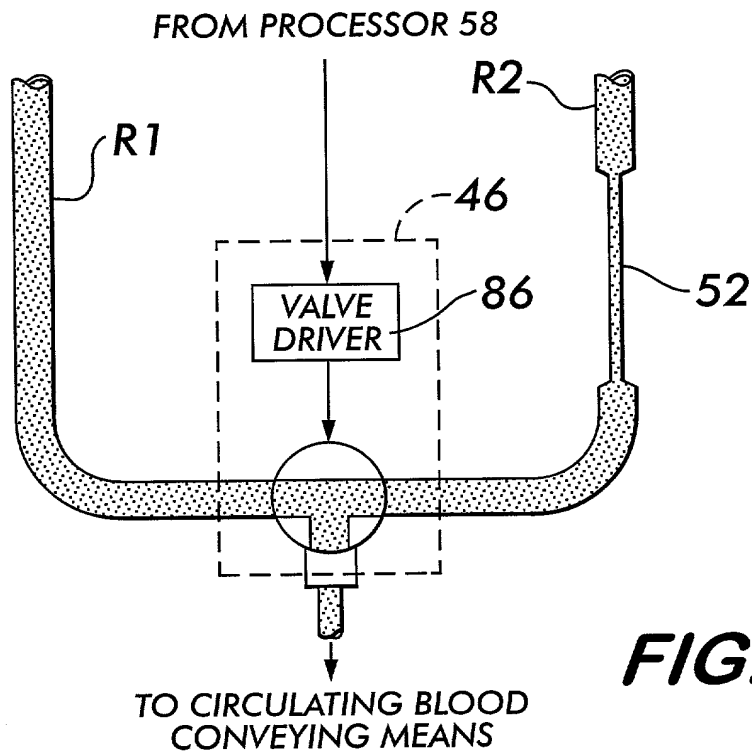
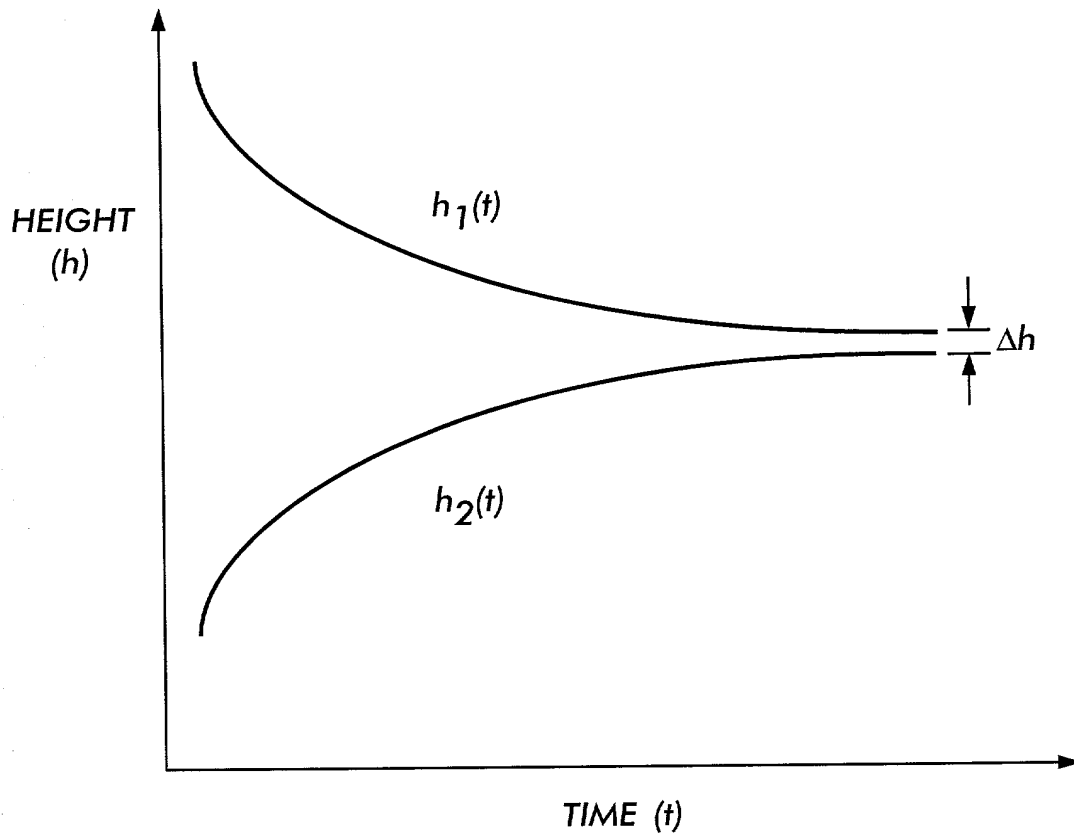
**FIG. 4**



**FIG. 5**



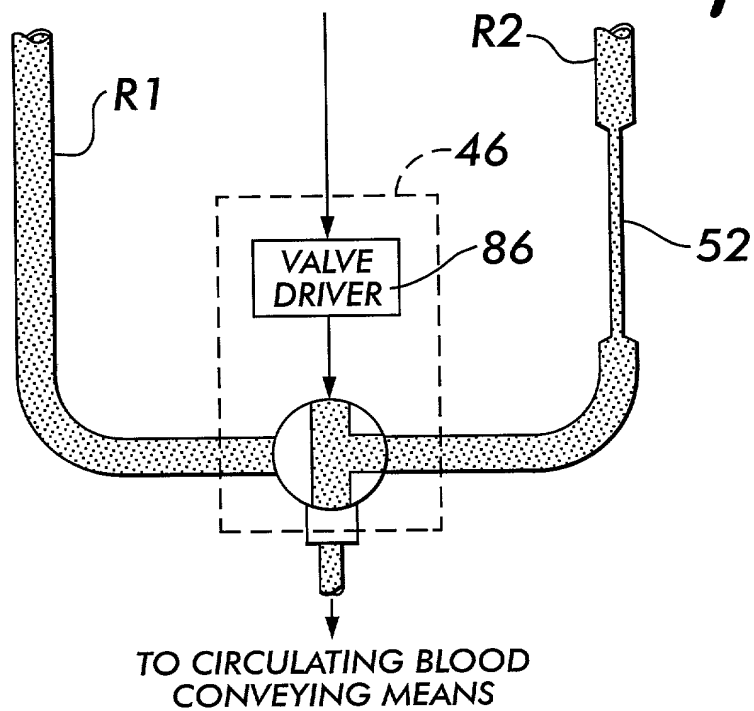
**FIG. 6**



**FIG. 7A**

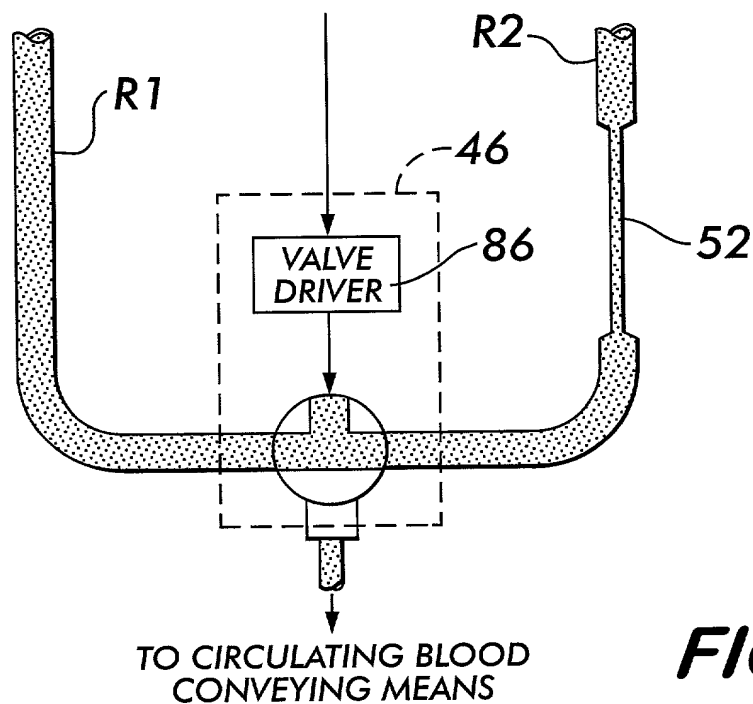
FROM PROCESSOR 58

**FIG. 7B**

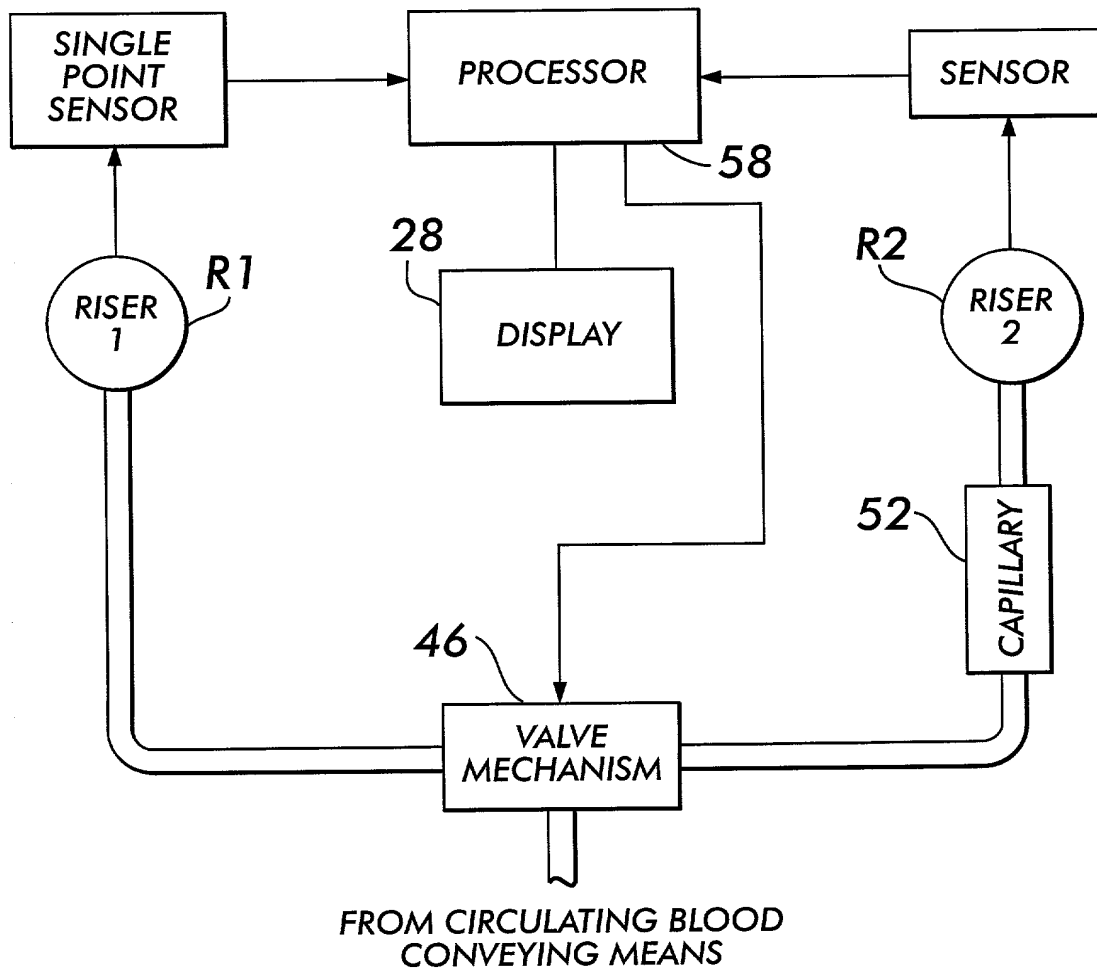


FROM PROCESSOR 58

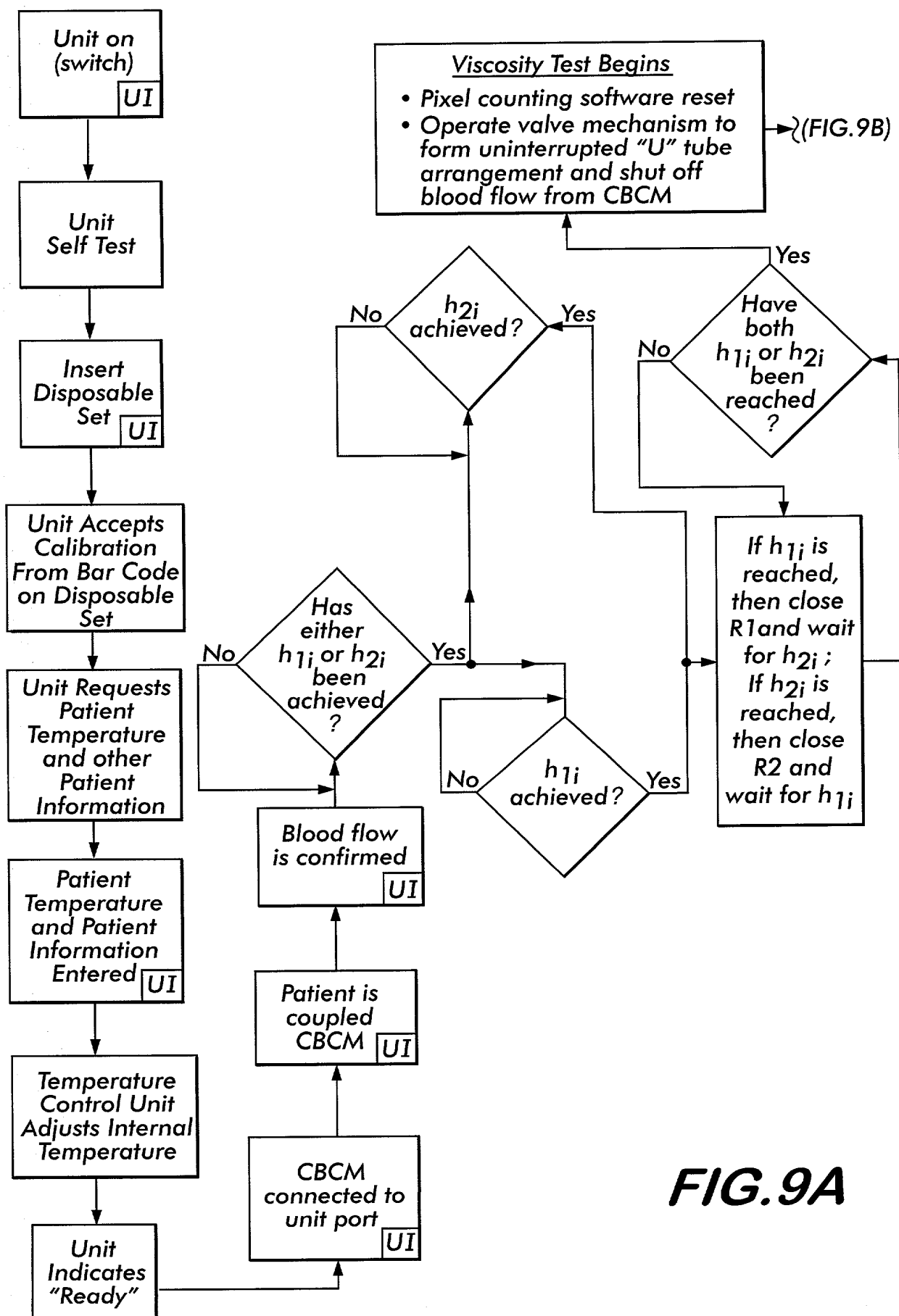
**FIG. 7C**

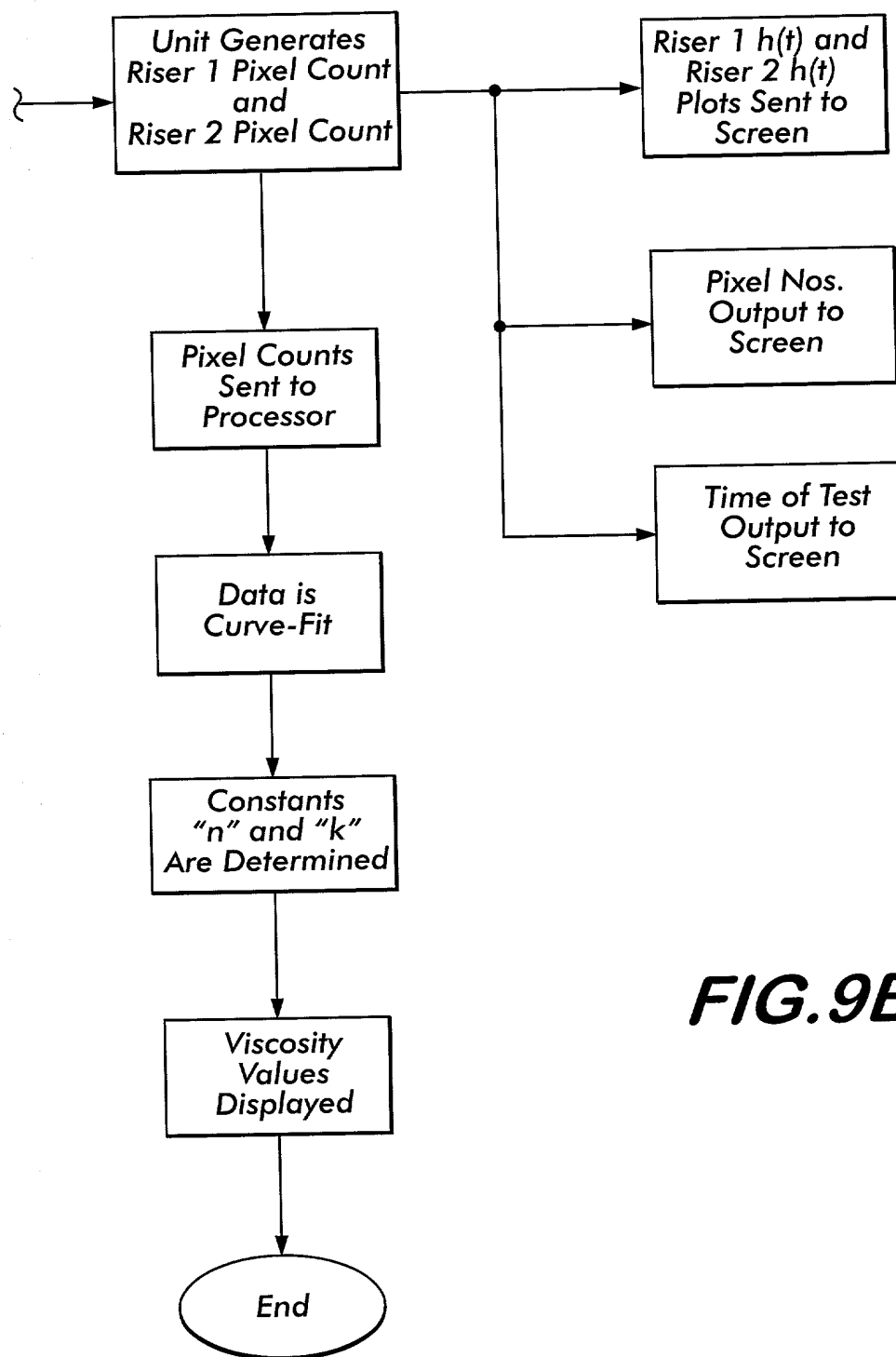


**FIG. 8**

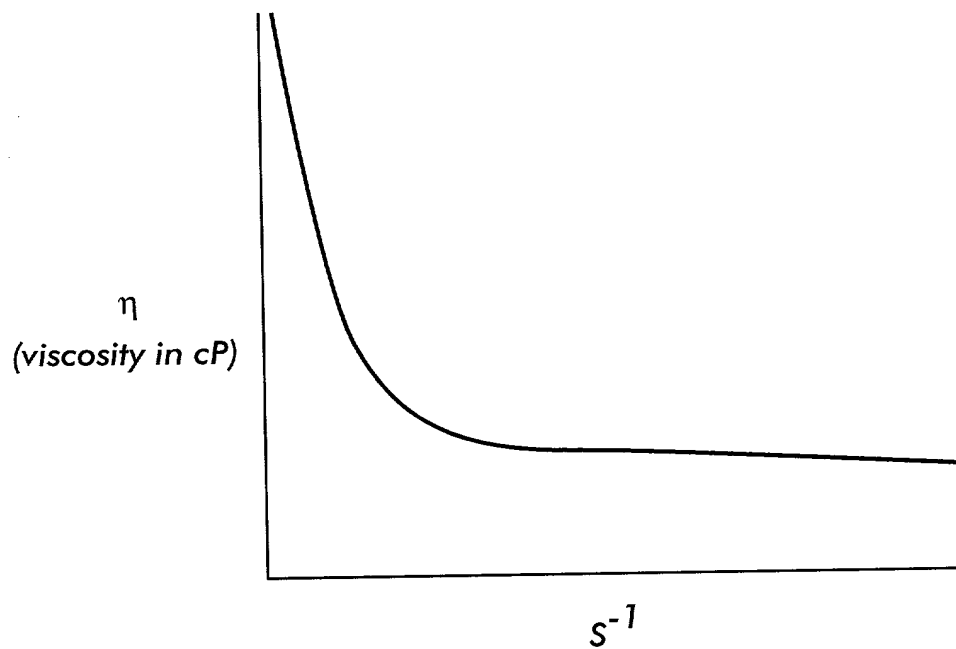




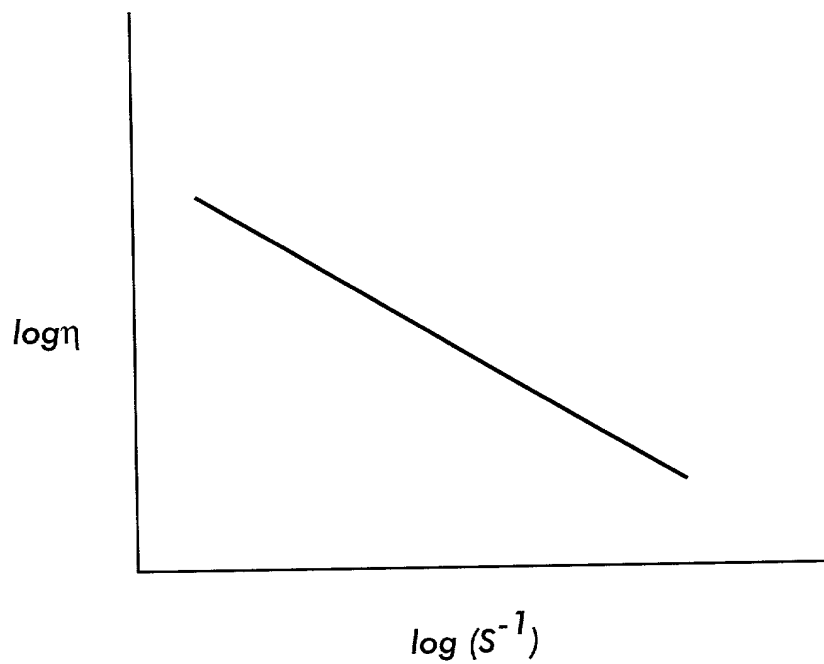




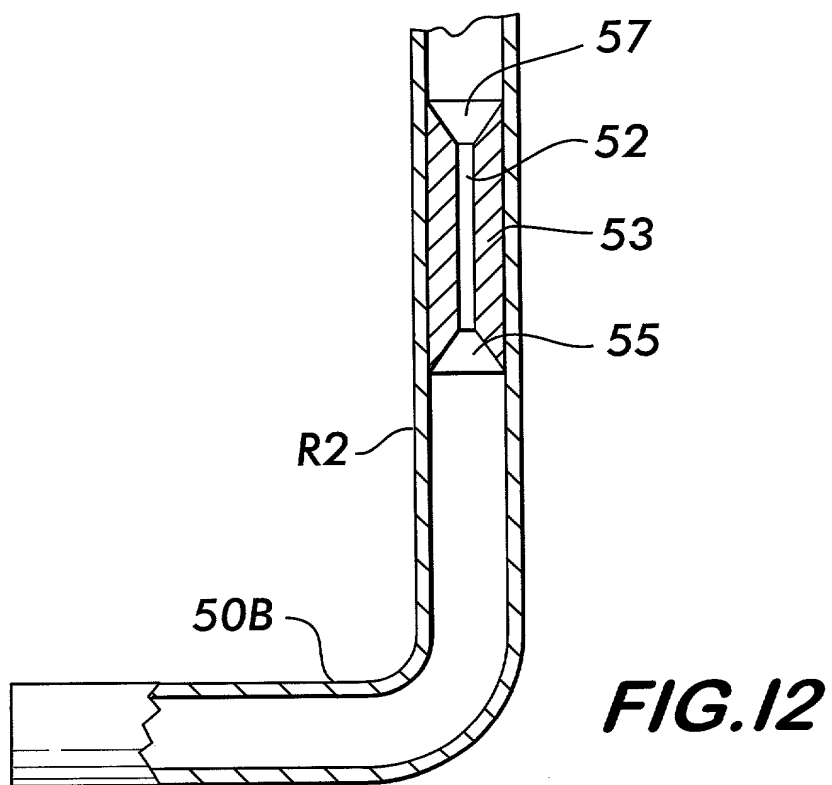
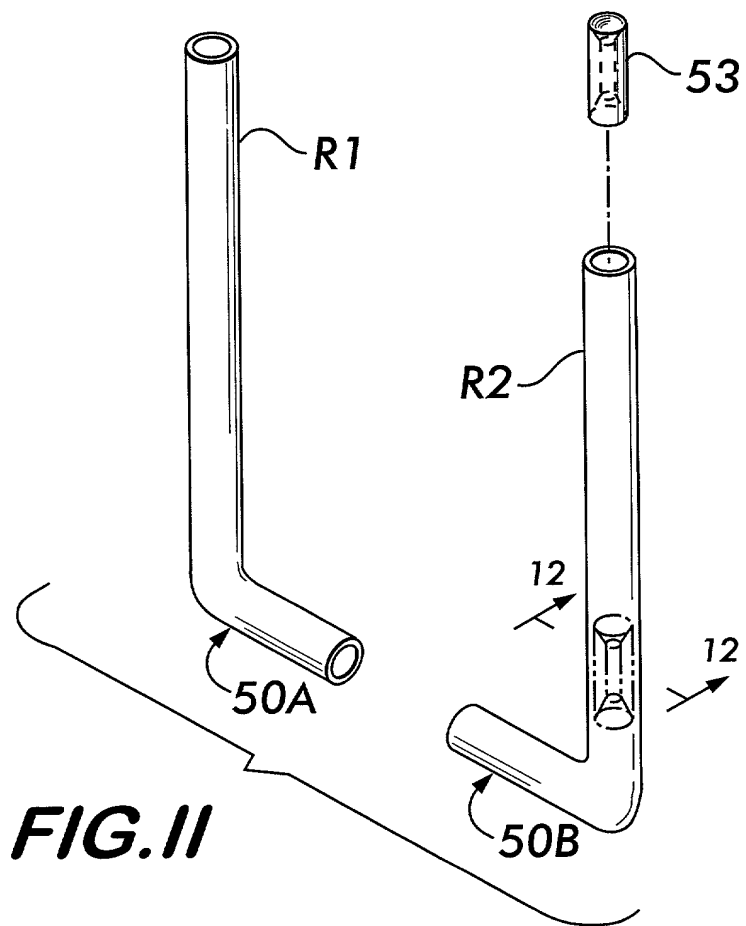
**FIG.9B**



**FIG.10A**



**FIG.10B**



# FIG. 13

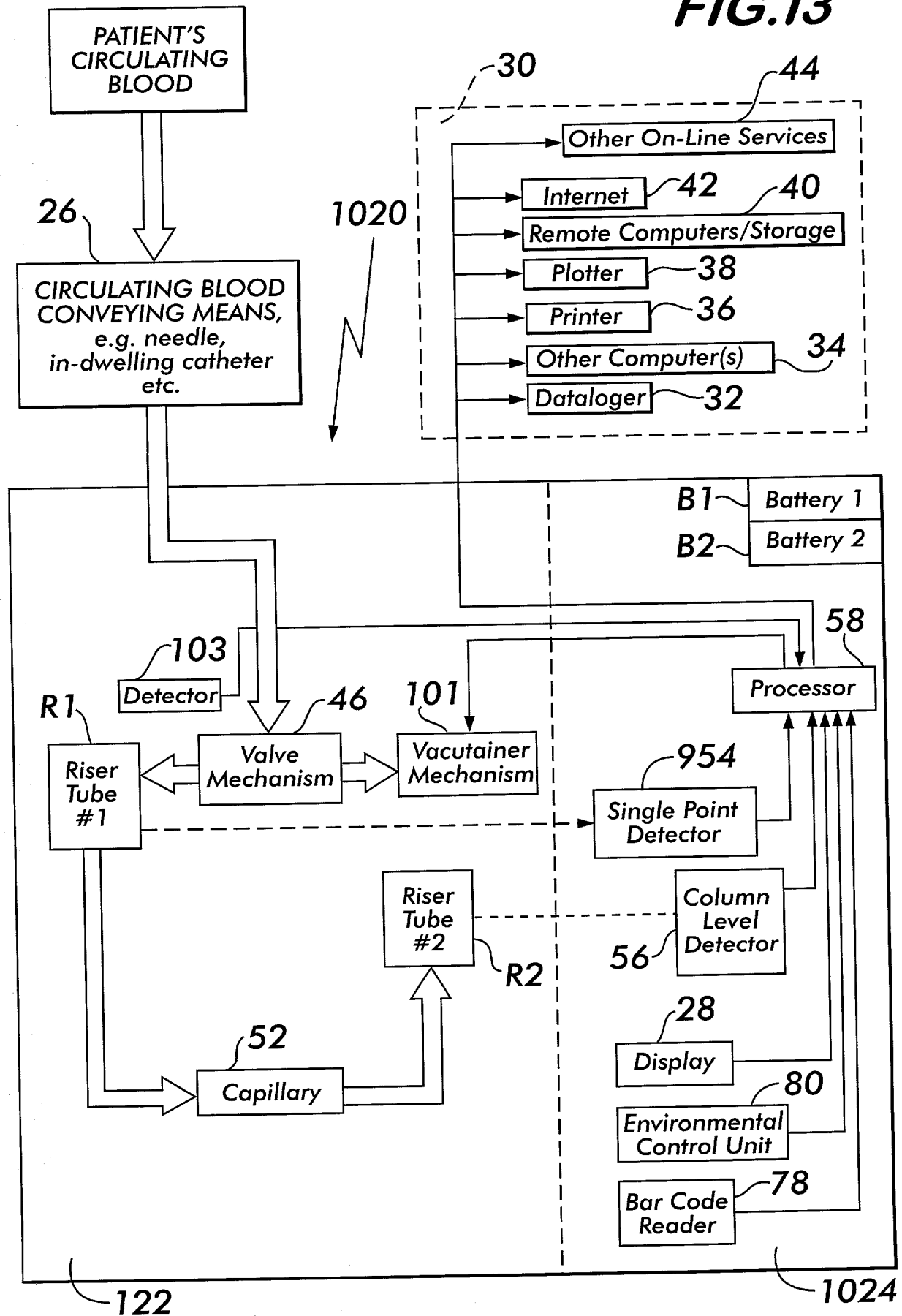
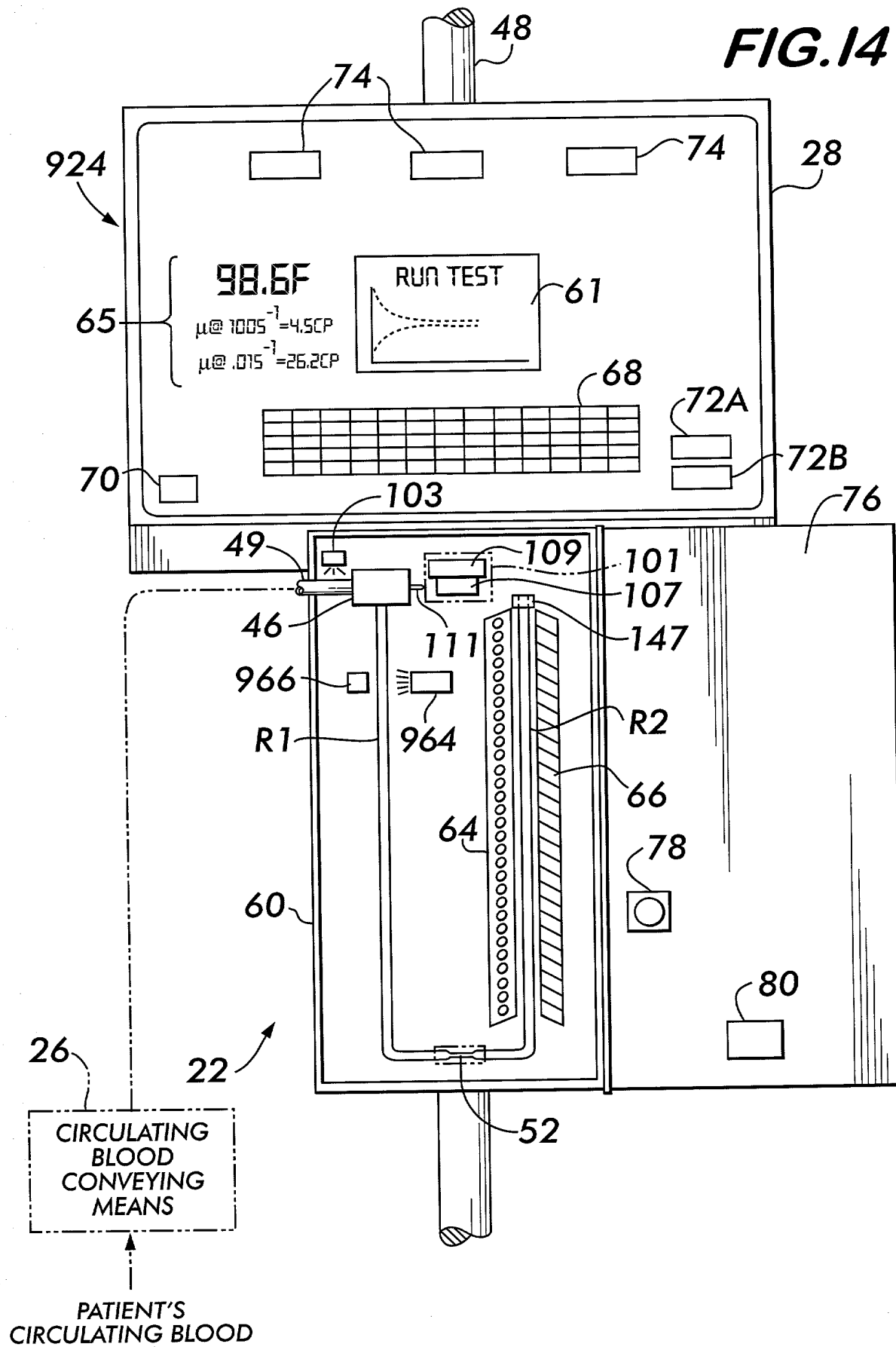
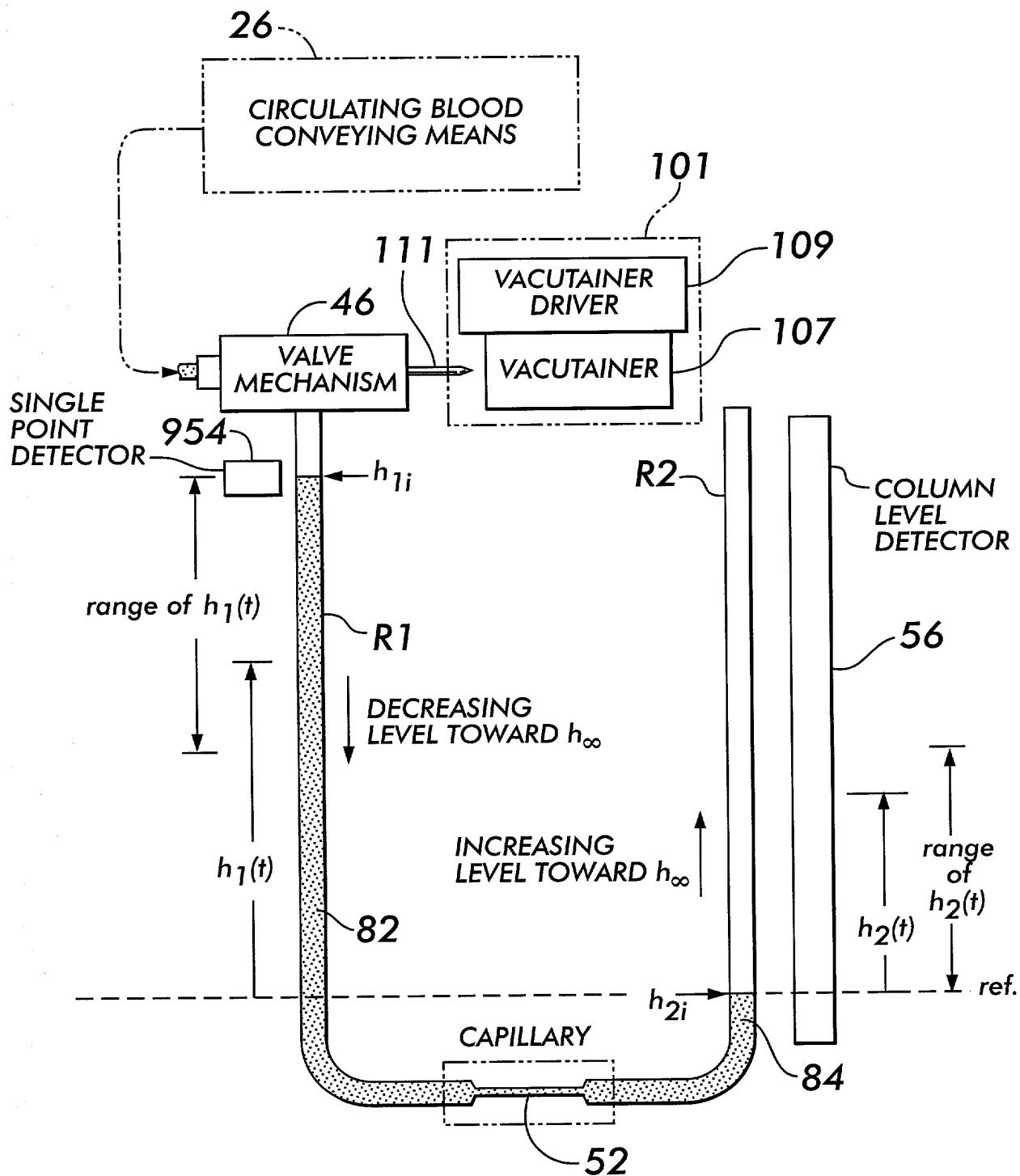


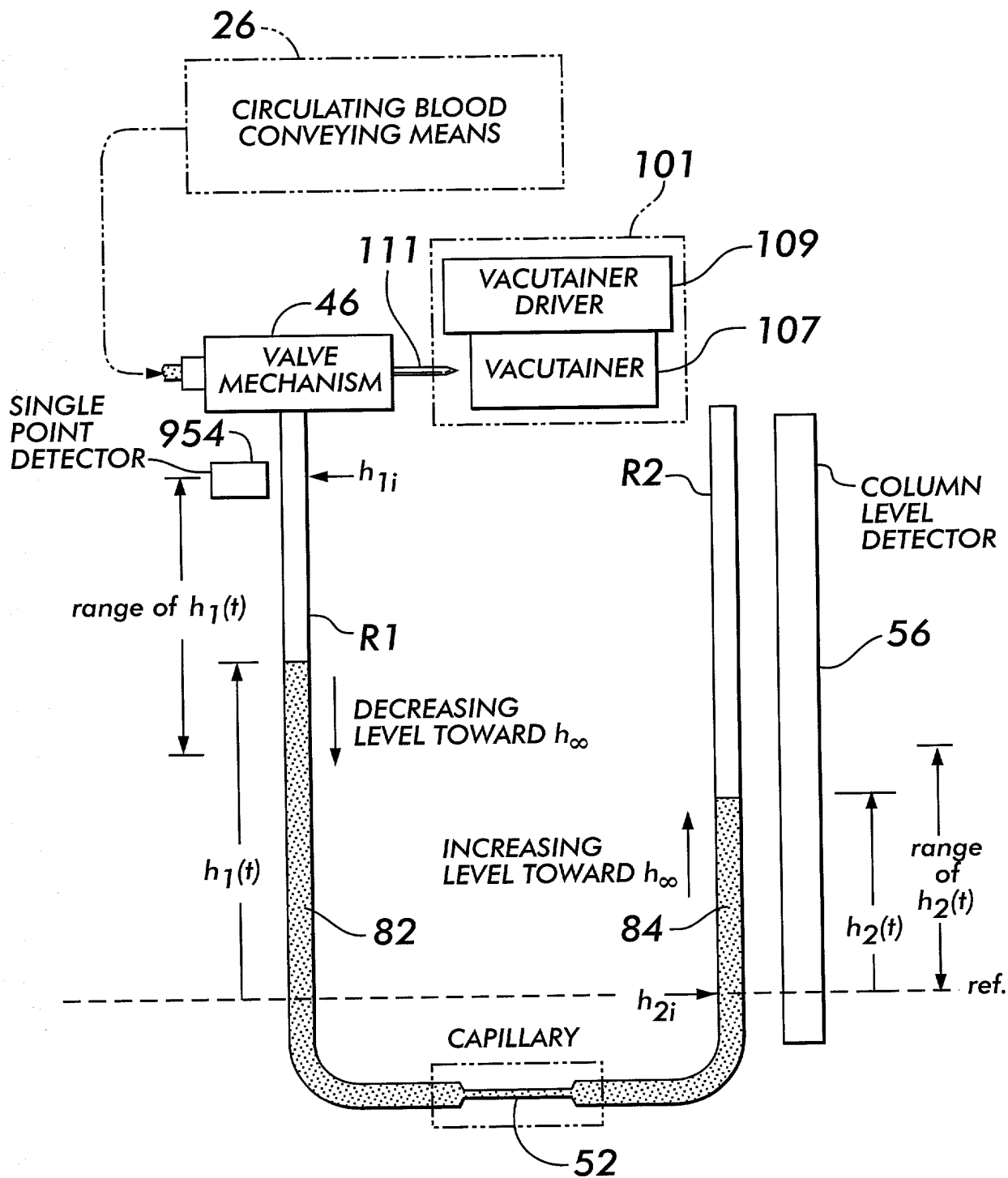
FIG. 14



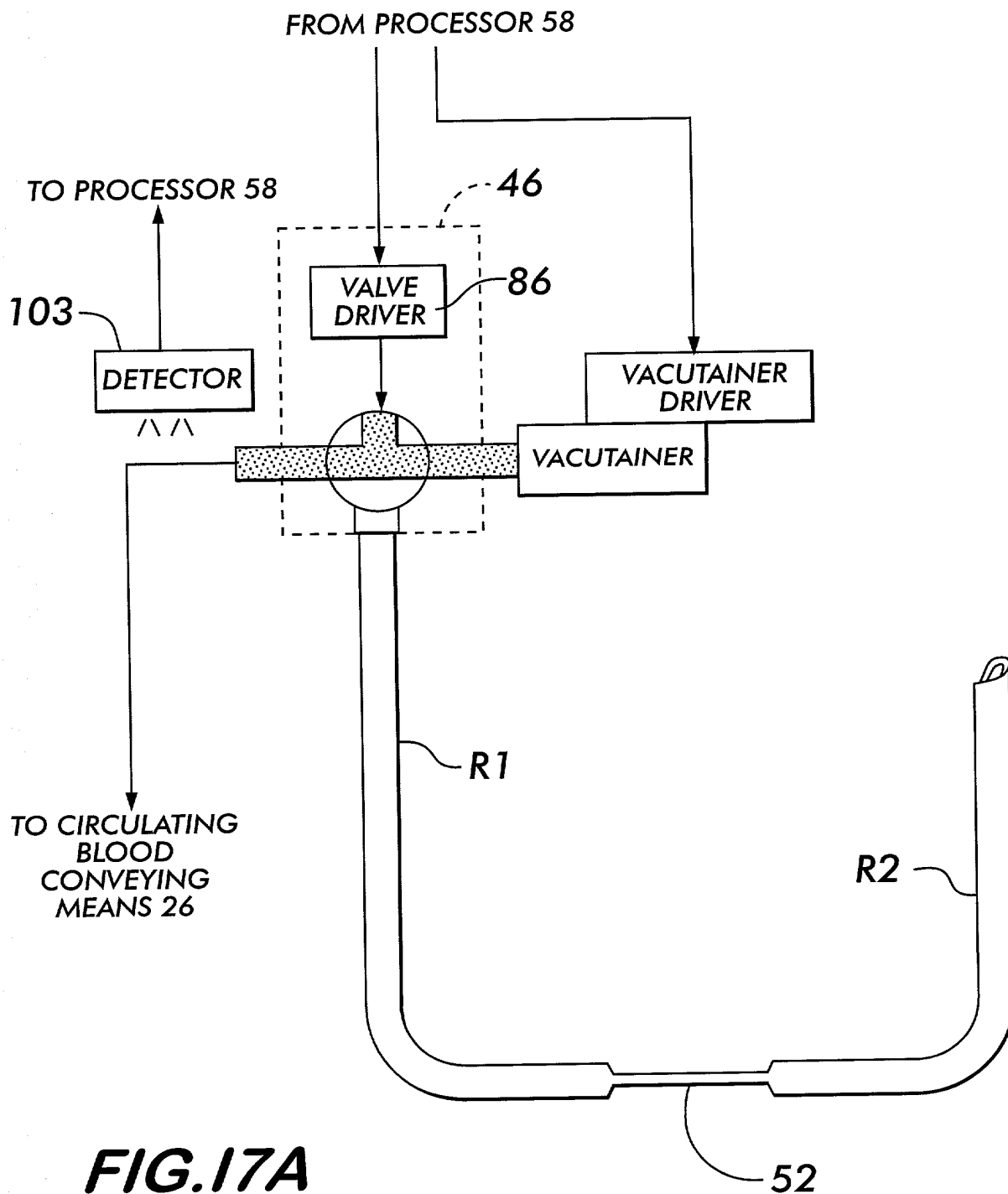
**FIG.15**

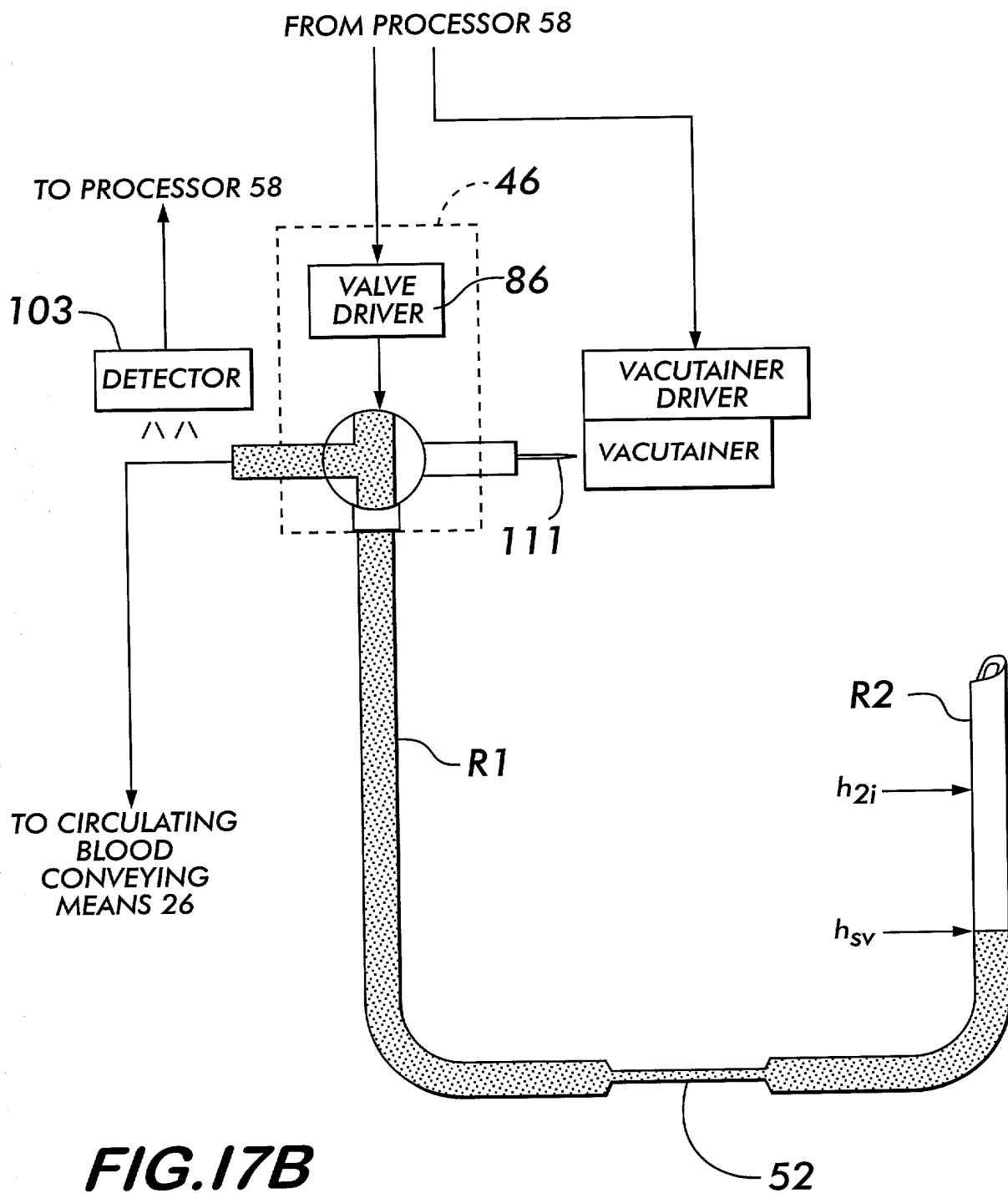


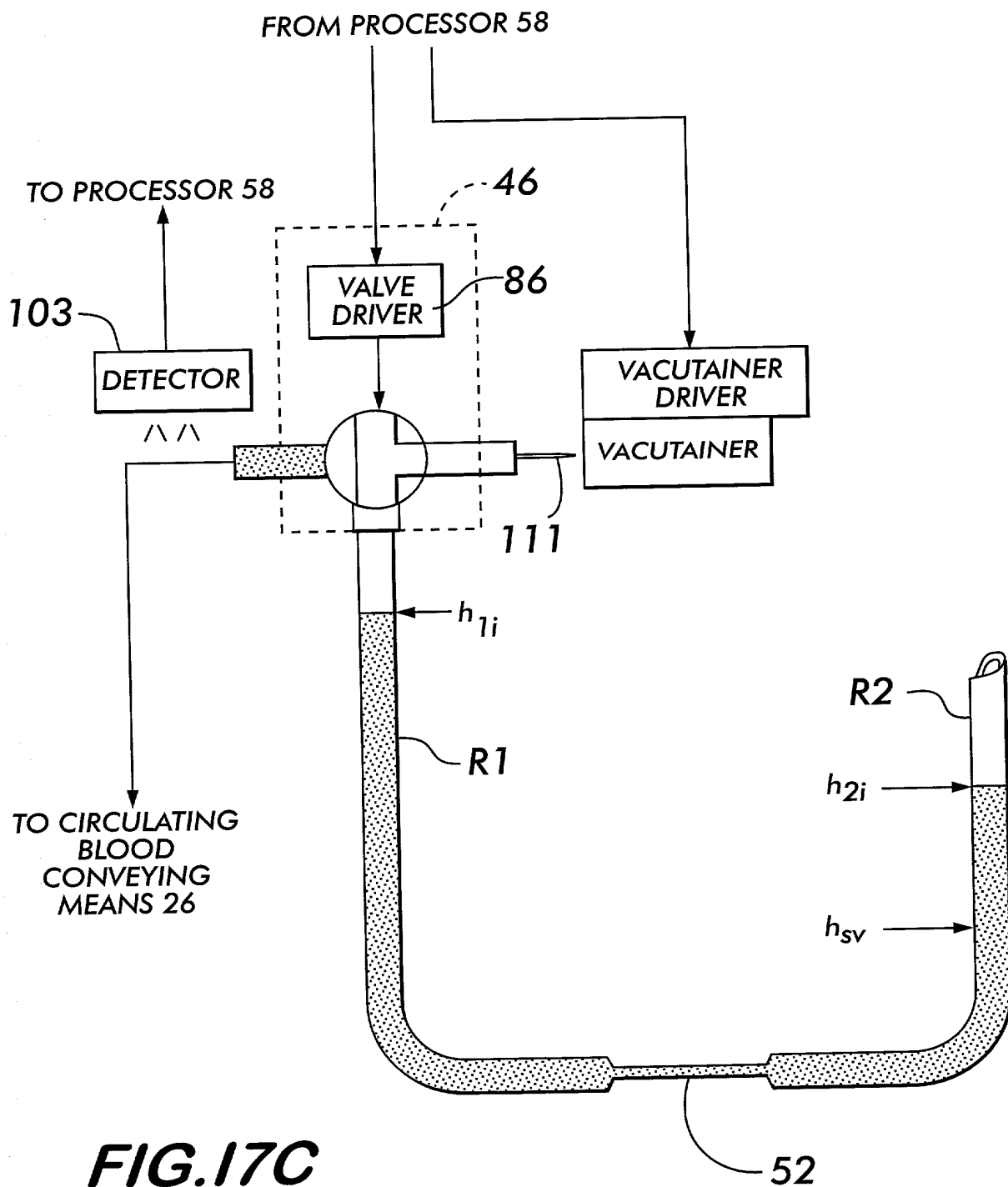
**FIG. 16**





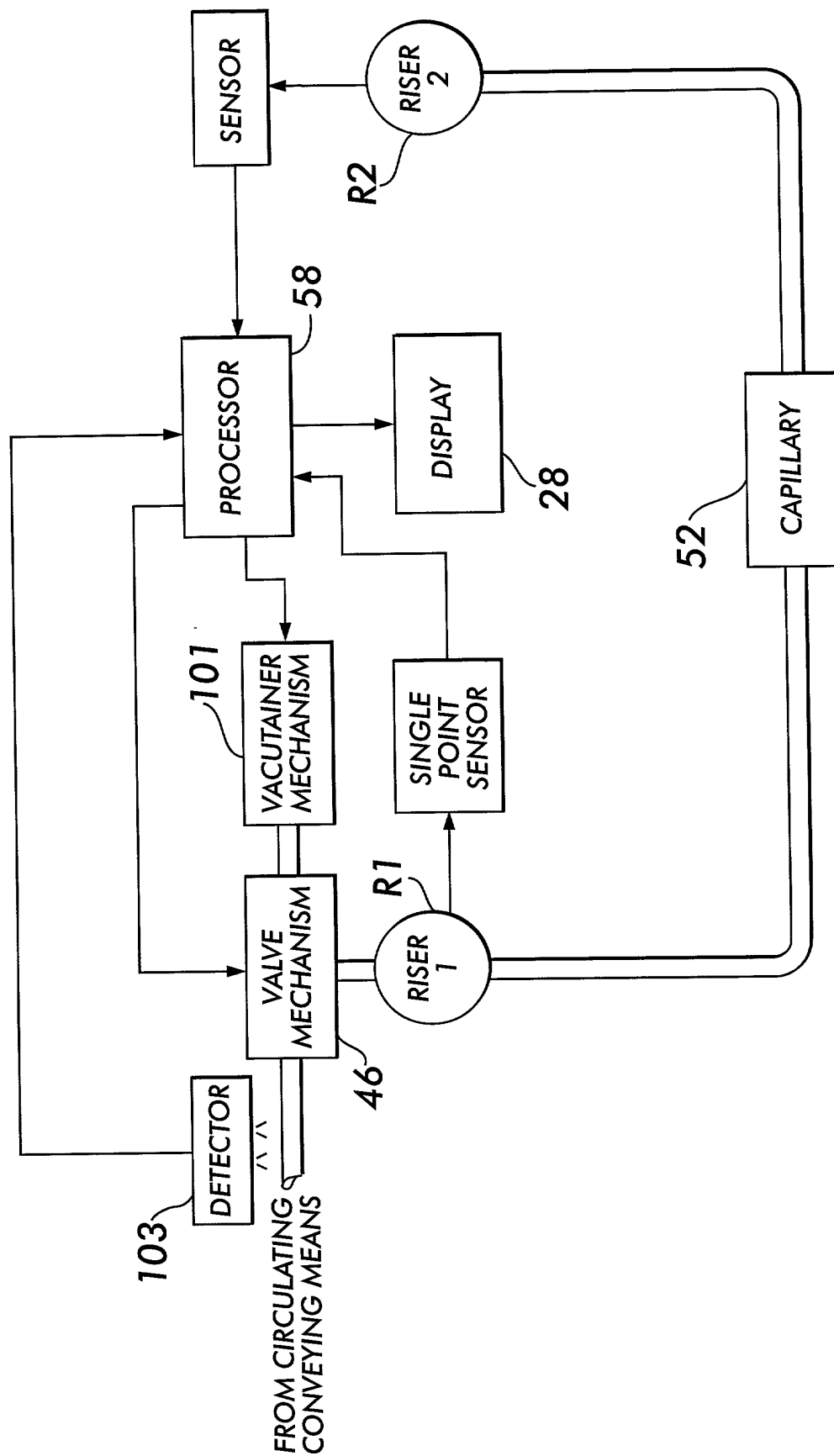




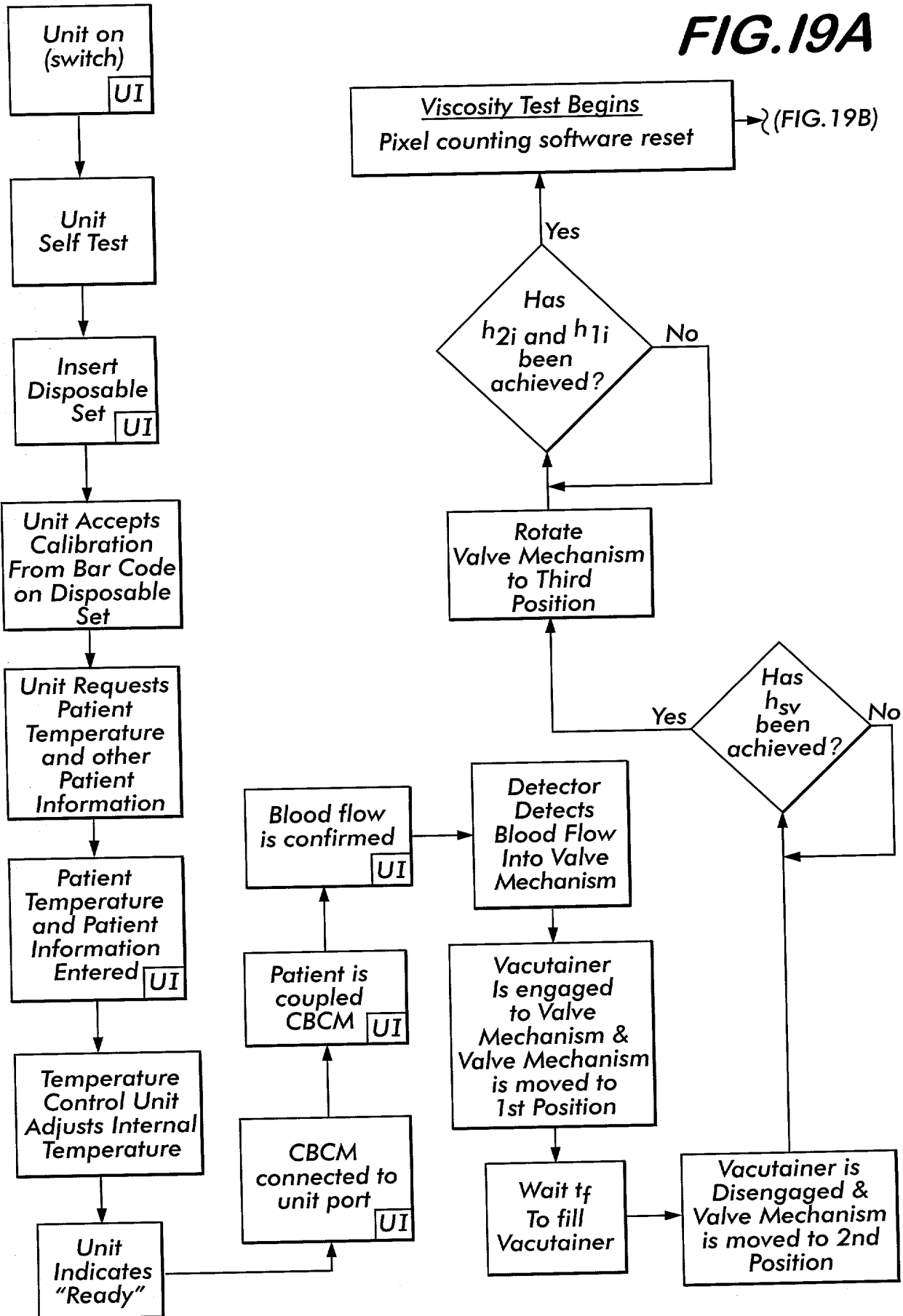


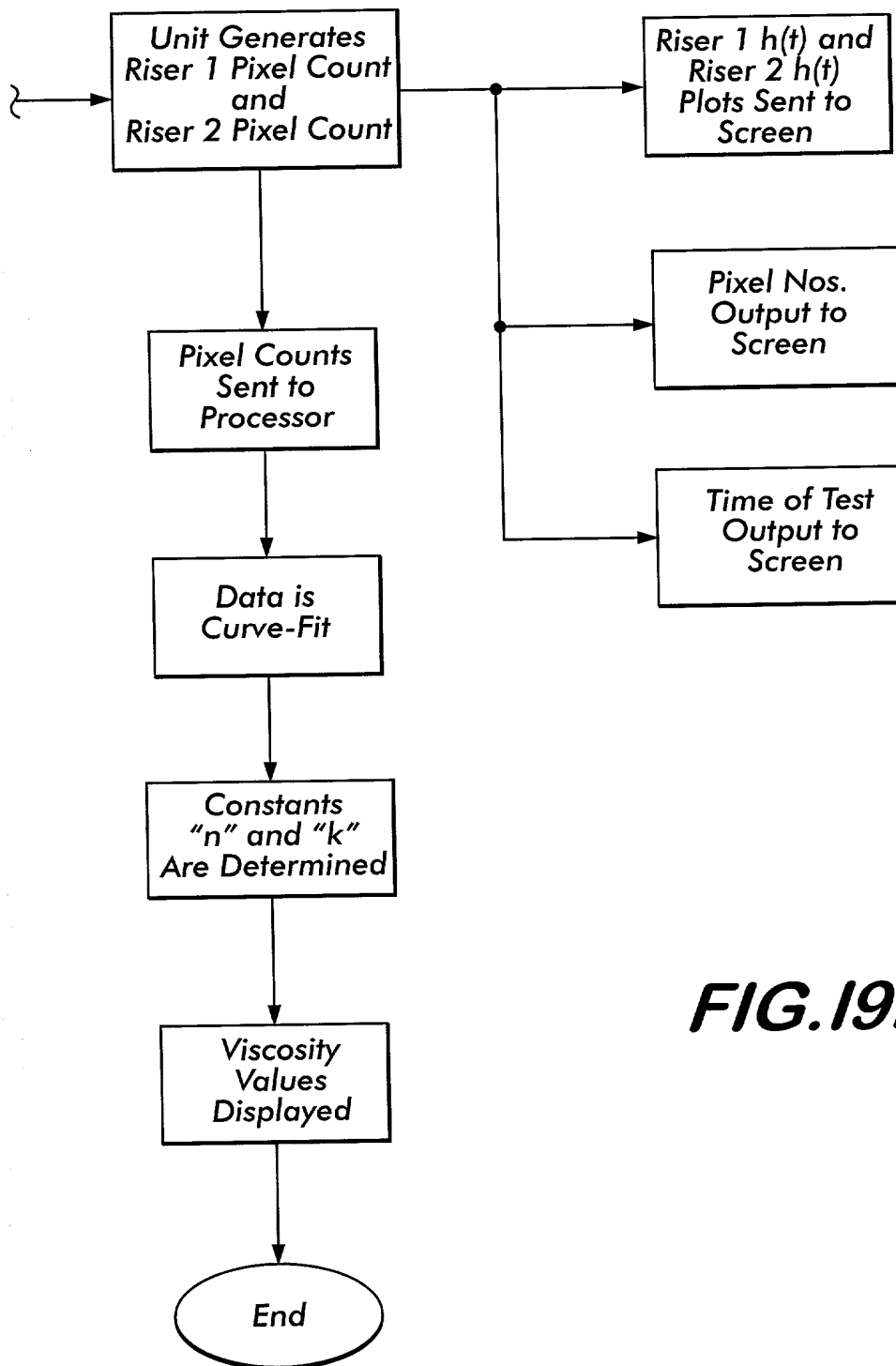
**FIG.17C**

FIG.18



**FIG.19A**





**FIG.19B**

